AMENDMENTS TO THE CLAIMS

1. (Previously Presented) A method of eliminating faulty memory cells from an active part of a memory array, the method comprising the steps of:

determining if cells in each column group of the memory array are defective;

configuring column groups of said memory array to replace ones of said column groups which include more than a predetermined number of defective cells with spare column groups by using bit line multiplexers to shift in a replacement column group of memory cells into said array;

identifying by row remaining defective cells not replaced by said step of configuring column groups of said memory array; and

configuring rows of said memory array to replace ones of said rows including said remaining defective cells.

2. (Original) The method of claim 1 wherein said step of determining includes the step of testing memory cells of said memory array to identify defective cells and counting a number of said defective cells identified in each of said column groups.

3. (Original) The method of claim 2 wherein said step of counting includes setting a threshold and counting said defective cells up to said threshold.

4. (Original) The method of claim 1 wherein said step of determining if cells in each column group of the memory array are defective further comprises the steps

generating at least one memory address;

writing data to a memory cell at said one memory address;

reading said data from said memory cell at said memory address; and

comparing said data written to said memory cell at said memory address with said data read from said memory cell at said memory address.

5. (Previously Presented) The method of claim 1 wherein the step of configuring rows of said memory array includes the step of translating a row address signal designating said ones of said rows including said remaining defective cells to instead select one or more spare rows of memory cells.

6. (Original) The method of claim 1 wherein the step of identifying said remaining defective cells includes the step of testing said memory array after performing said step of configuring said column groups.

7. (Original) The method of claim 1 wherein said step of determining is performed by built in self test.

8. (Original) The method of claim 1 wherein said steps of configuring column groups and configuring rows are performed by built in self repair.

9. (Previously Presented) A system for eliminating faulty memory cells from a memory array comprising:

a memory cell tester for determining non operational cells;

a column group reconfigurer for replacing ones of said column groups which contain a predetermined number of non operational cells, said column group reconfigurer including bit line multiplexers to shift in a replacement column group of memory cells into said array;

a remaining non operational cell identifier which identifies remaining non operational cells in said memory array; and

a row reconfigurer for replacing ones of said rows which contain non operational cells.

10. (Original) The system of claim 9 wherein said memory cell tester further counts the number of non operational cells in each of the column groups.

11. (Original) The system of claim 10 wherein said memory cell tester includes a threshold and counts the number of non operational cells up to said threshold.

12. (Original) The system of claim 9 wherein said memory cell tester further comprises:

a memory cell test data generator configured to write values in said memory cell;

a memory cell data output configured to read values from said memory cell;

a first register configured to store the value written into said memory cell;

a comparator configured to compare said value stored in said first register with said value read from said memory; and

a second register configured to record a result from said comparator.

13. (Previously Presented) The system of claim 9 wherein said row reconfigurer further includes a row address signal which selects one or more spare rows of memory cells.

14. (Original) The system of claim 9 further comprising:

a semiconductor substrate; and

a memory array found on a portion of said semiconductor substrate; where said memory cell tester, column group reconfigurer, remaining cell identifier and row reconfigurer are all formed in common with said memory array on said semiconductor substrate.

15. (Original) The system of claim 14 further comprising built in self test and built in self repair.

16. (Previously Presented) A method of eliminating faulty memory cells from a memory array, the method comprising the steps of:

determining if cells in each row of the memory array are operational;

configuring rows of said memory array to replace ones of said rows which include a predetermined number of non operational cell with spare rows by activating an alternate word line to shift in a replacement row of memory cells into said array;

identifying remaining defective cells not replaced by said set of configuring rows of said memory array; and

configuring column groups of said memory array to replace ones of said column groups including said remaining defective cells,.

17. (Original) The method of claim 16 wherein said step of determining includes a step of testing memory cells of said memory array to determine defective ones of said cells and counting said defective cells in each of the rows.

18. (Original) The method of claim 17 wherein said step of counting includes setting a threshold and counting said defective cells up to said threshold.

19. (Original) The method of claim 16 wherein said step of determining if cells in each row of the memory array are operational further comprises the steps of:

generating at least one memory address;

writing data to at least one memory cell at said memory address;

reading said data from said memory cell at said memory address; and

comparing said data written to said memory cell at said memory address with said data read from said memory cell at said memory address.

20. (Previously Presented) The method of claim 16 wherein the step of configuring column groups includes translating a column address signal designating said ones of said columns including said remaining defective cells to instead select one or more spare columns of memory cells.